AMENDMENT TO THE CLAIMS:

Claims 1-4 (Canceled)

Claim 5. (Currently Amended) A memory, comprising:

a gate conductor comprising a first side and a second side~~s~~, said first side comprising a slope and said second side comprising a substantially vertical sidewall; and

at least one floating gate comprising polysilicon spacer material and formed on said second side of said gate conductor such that said gate conductor surrounds said at least one floating gate on a plurality of sides,

wherein said slope comprises an angle of taper between about 45^0 and about 65^0.

Claim 6. (Previously Presented) The memory according to claim 5, wherein said gate conductor is formed on a silicon substrate, and

wherein adjacent ones of said at least one floating gate are isolated from each other and said second side includes tapered regions provided between the adjacent ones of said at least one floating gate.

Claim 7. (Original) The memory according to claim 5, wherein said gate conductor surrounds said at least one floating gate on only two sides.

Claim 8. (Original) The memory according to claim 5, wherein said gate conductor surrounds said at least one floating gate on at least two sides.

Claim 9. (Original) The memory according to claim 8, wherein said gate conductor surrounds said at least one floating gate on three sides.

Claim 10. (Original) The memory according to claim 5, wherein said at least one floating gate is self-isolated from an adjacent floating gate by said gate conductor.

Claim 11. (Original) The memory according to claim 10, wherein said gate conductor surrounds said at least one floating gate on at least two sides.

Claims 12-49. (Canceled)

50. (Previously Presented) The memory according to claim 5, wherein said floating gate formed on said gate conductor comprises a single sidewall structure.

51. (Previously Presented) The memory according to claim 5, further comprising a source and a drain each formed and aligned on a same level.

52. (Previously Presented) The memory according to claim 5, wherein said gate conductor comprises a control gate.

53-54. (Canceled)

55. (Previously Presented) The memory according to claim 5, wherein said first side comprises a tapered sidewall.

56. (Previously Presented) The memory according to claim 5, further comprising an oxide layer formed on said second side and having a substantially uniform thickness.

57. (Previously Presented) The memory according to claim 5, further comprising a tunneling region formed underneath said floating gate.

58. (Previously Presented) The memory according to claim 5, wherein said gate conductor is covered by a dielectric comprising a thickness in a range of about 100 nm to 1,000 nm.

59. (Previously Presented) The memory according to claim 5, wherein said second side comprises a notch side having three sidewalls, said floating gate being formed on said three sidewalls.

60. (Previously Presented) The memory according to claim 5, wherein said gate conductor comprises an active area, and

wherein said floating gate overlaps said active area by a predetermined minimum

dimension to provide a predetermined threshold voltage.

61. (Previously Presented) The memory according to claim 5, wherein an oxide sidewall is formed on said gate conductor.

62. (Currently Amended) A memory, comprising:

a gate conductor comprising a first side and a second side, said first side comprising a first slope and said second side comprising a second slope, where said second slope is greater than said first slope; and

a floating gate formed on said second side of said gate conductor such that said gate conductor surrounds said at least one floating gate on a plurality of sides,

wherein said first slope comprises an angle of taper between about 45^0 and about 65^0.